Amendments to the Specification:

Please replace the paragraph beginning at page 32, line 36, with the following rewritten paragraph:

The error data output via the terminals "a", "b", and "c" and "d" are fed to the adder 32a, an adder 35a, and an adder 34a, respectively. The adder 34a adds the error data from the terminals "d" and "c". The output of the adder 34a is fed to the adder 35a and added to the error data from the terminal "b". The addition result is fed to a line memory ~~360a~~ 36a by which the output of the adder ~~350~~ 35a is delayed by a period slightly shorter than a period for one line and fed to the adder ~~310a~~ 31a.

Please replace the paragraph beginning at page 33, line 7, with the following rewritten paragraph:

The output of the line memory ~~360a~~ 36a and the input R(G or B)-signal are added by the adder 31a and fed to the adder 32a. The input R(G or B)-signal corresponds to the dot P' in FIG. 21 in this embodiment. The adder 31a performs addition of the output of the line memory 36a that is the error data generated one line ago to the ~~to the~~ dot P', or B' x 3/16 + C' x 5/16 + D' x 1/16.